AYDIN CONTROLS

414 COMMERCE DRIVE, FORT WASHINGTON, PA 19034

OPERATION & MAINTENANCE MANUAL

For

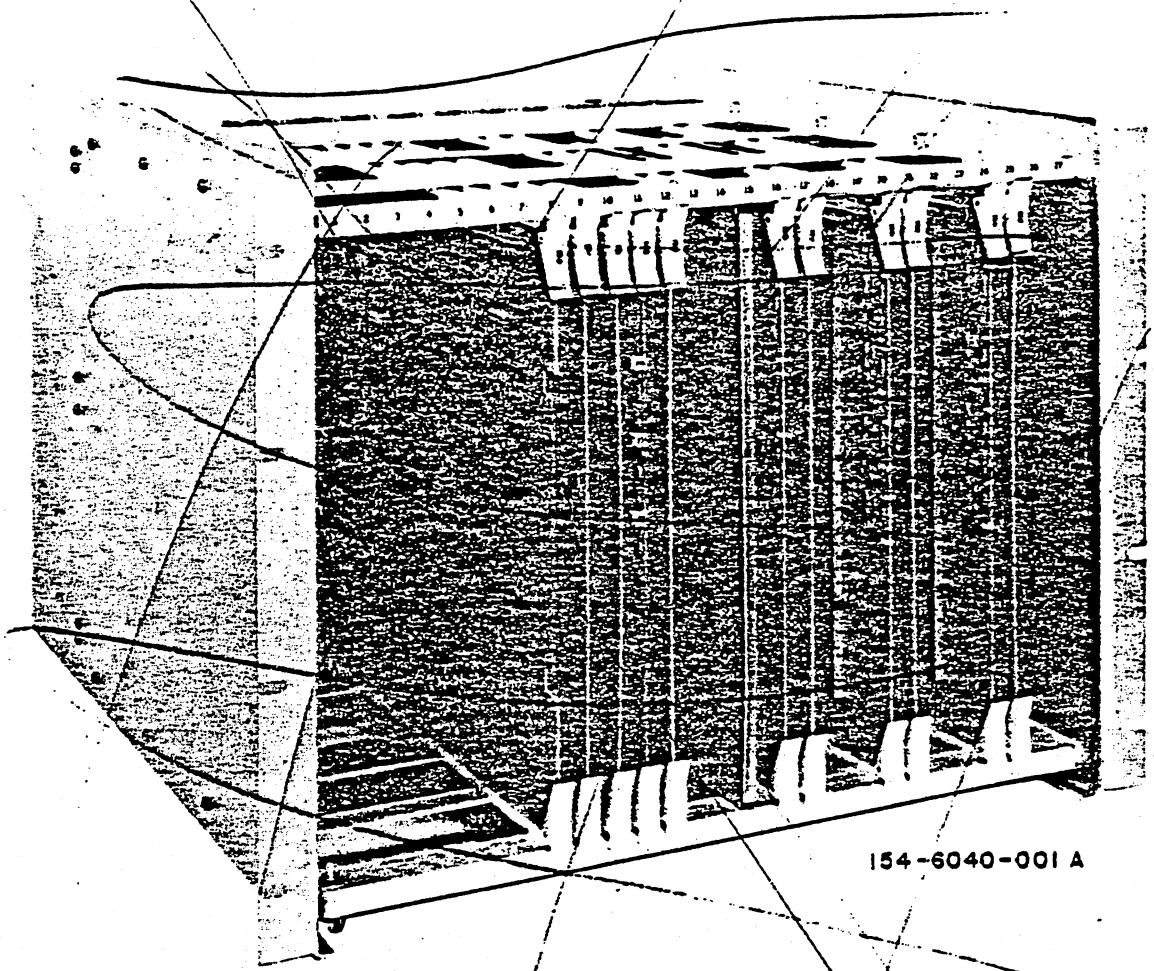
HPV-2 MODEL 5215 DISPLAY GENERATOR

Document AR94-V-O&M

May 1977

NOTE

This manual is a modified version of AYDIN CONTROLS document 150-6040-001A, reflecting the options supported by Honeywell in the HPV-2 Video Display Subsystem used on HS4400 and TDC 4500 Process Computer Systems. Due to the complexity of the subsystem it is not possible to troubleshoot and repair this equipment in the field through logic and circuit analysis. Therefore, troubleshooting and repair will be done only through board and subassembly replacement, hence, engineering logic drawings and printed circuit board drawings and parts lists are not included in this documentation.



5215 DISPLAY GENERATOR

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Volume I

CHAPTER 1

GENERAL INFORMATION AND DESCRIPTIONS

1.1 RELATED SUPPORTING PUBLICATIONS

1.1.1 Breakdown of Supporting Publications

The AYDIN CONTROLS Model 5215 Display Generator Manual consists of three (3) Volumes:

Volume I	Operation and Maintenance Manual (Document AR94-V-O&M)
Volume II	Data Flow Block Diagrams, Engineering Logic Drawings and Wiring Lists (Document AR94-V-EDWG)
Volume III	Programming Information (Document PTS-036)

NOTE: Supporting documents for the 5115 Display Editor (an option for use with the 5215 Display Generator) include:

Volume I	Operation and Maintenance Manual (Document AR54-V-O&M)
Volume II	Data Flow Block Diagrams and Engineering Logic Drawings (Document AR54-V-EDWG)

This document, Volume I for the 5215 Display Generator, is intended for use as a hardware maintenance guide. It includes separate sections which describe the general to detailed hardware architecture, hardware nomenclature and theory of operation. Maintenance procedures, including special tools and recommended test equipment, are also listed within.

Chapters 1 through 5 of this Volume (Volume I) relate only to the Standard Display Generator. Chapter 6 defines some of the available options and their related effect on what is otherwise considered standard.

1.1.2 Reference From Volume I to Volume II

Throughout this Volume, the reader will want to refer to supporting Data Flow Charts in Volume II. Starting from the Master Data Flow Block Diagram in Volume II, it is easy to find the way, step-by-step, to progressively more detailed drawings in Volume II.

Each "Card" section of the Master Data Flow Block Diagram (Volume II) has a "blocked" number, normally in the upper right hand corner. This number refers to the more detailed Block Diagram for that particular card. The same blocked number will appear in the right hand corner of the title block of the detailed Block Diagram referenced.

1.2 FUNCTIONAL DESCRIPTION OF I/O, TVD-193

The AYDIN CONTROLS Model 5215 Display Generator is an electronics subsystem which processes digital data for Color Cathode Ray display purposes. Refer to Master Data Flow Block Diagram in Volume II. It interfaces directly to a computer(s) for the purpose of receiving and/or transmitting either parallel or serial control and display data. Local operator control, display data entry and interrupt generation is accomplished with the use of a compatible AYDIN CONTROLS Display Editor (keyboard), Model 5115. Once the Display Generator receives a command to write display data on a CRT Monitor, it will maintain that data until a change is commanded by either of the two data/control sources (Computer or Keyboard).

The Display Generator is capable of transferring the character display data and the status that it maintains to the computer upon computer command. Interrupt signaling and interrupt status may also be transferred to the computer in order to provide for operator/computer interactive display and control operations.

The horizontal configuration Display Generator (Model 5125P-2) is designed to drive from one (1) to four (4) CRT Monitors, operating from one (1) or two (2) computer inputs. Computer inputs may be either serial or parallel type, depending on the I/O Card used.

1.2.1 General Logic Card Functions

The Display Generator logic hardware is functionally divided into three main sections. Interface, Common Control Logic and Standard Display Logic. Basic descriptions of these sections are given in the following text. Refer to the Master Data Flow Block Diagram in Volume II for the following discussion.

1.2.1.1 Interface

I/O Card (interface) TVD-193 provide the data transfer and control link required to interface a computers general purpose I/O port to the 5215 Control Card (Processor) TVD-194. The I/O Card converts data transfer and control line signals from either of the two sources (computer and display generator) to be compatible to operation signals to either of the two destinations. Computer I/O control and data lines may be bussed to include multiple Display Generators on the same computer I/O port (parallel data input only).

The I/O Card TVD-193 may be used for either serial or parallel input/output; factory-wired for either.

Single Computer Input - for single computer input, the following logic cards are required:

1-4 Channel Set, TVD-190 and TVD-192
1 Sync Card, TVD-191
1 Control Processor Card, TVD-194
1 I/O Card (Interface), TVD-193 (serial or parallel I/O)

Dual Computer Input - for dual computer input, the following logic cards are required:

1-4 Channel Set, TVD-190 and TVD-192
1 Sync Card, TVD-191
2 Control Processor Cards, TVD-194
2 I/O Cards (Interface), TVD-193 (dual serial or dual parallel I/O)

1.2.1.2 Common Control Logic

The common control logic is comprised of the Sync Generator Card (TVD-191) and the Control Card (TVD-194).

The Sync Generator provides both common and dedicated timing signals and time frame pulses to all Display Generator logic, thereby synchronizing I/O, internal data transfer, and video output operations.

The Control Card controls the majority of I/O transfers and control operations that occur to and from the Display Generator. I/O transfer display writing, reading and the editing of existing displays is controlled by an internal processor program that is accessed via communication message codes and code sequences.

1.2.1.3 Standard Display Logic

The Standard Display Logic is comprised of from one to four Standard Channel Sets. Each channel set is addressed as a separate Display Generator video channel for communication purposes and provides composite video signals to a color and/or a monochrome Cathode Ray Tube (CRT).

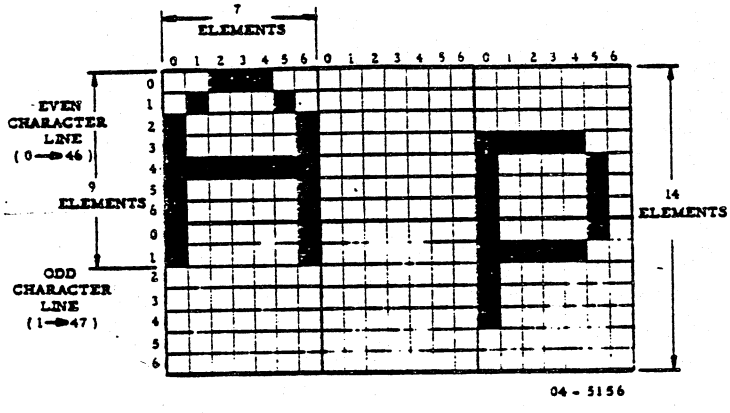
The Standard Channel Set is comprised of the Video Output Card (TVD-190) and the Edit Card (TVD-192). Under control of the Common Control Logic and the Edit Card, the Video Output card stores and processes internal memory data in order to drive color and monochrome CRT control outputs.

1.2.1.3.1 Page Display Characteristics

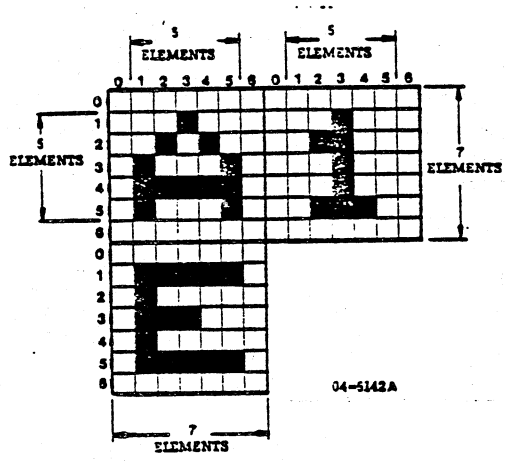
As depicted in the following illustration, the Standard Channel Set is designed to display both "Normal" and "Large" character configurations within a page matrix of 80 positions/line by 48 lines.

Under program control, an additional 4 lines termed the "Menu Area" may be displayed in lieu of the last four lines (44 through 47) of the normal page matrix (or vice-versa).

LARGE CHARACTERS



NORMAL CHARACTERS



1.2.1.3.2 Character Configurations and Attributes

Any one of 128 unique Normal Character configurations may be selected for display at any one of 3,840 positions within the page matrix.

128 unique Large Character configurations are also available to the user, but require 2 contiguous page matrix positions for display. Any one of the Large Character configurations may be selected for display anywhere within the page matrix with the restriction that the characters be written on a contiguous even-odd line pair for the top and bottom of the character respectively.

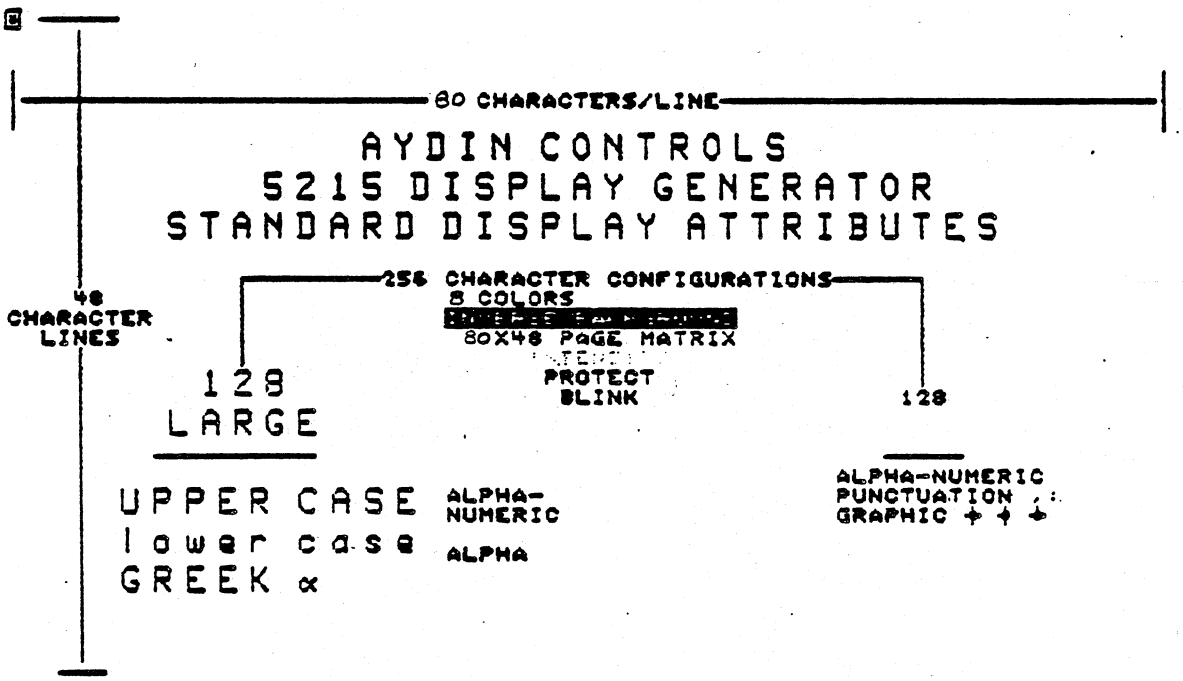
Each page matrix position is comprised of a fixed 7 x 7 element matrix in which certain elements are illuminated/not illuminated in order to display the preprogrammed character configurations.

Large Character configurations require one horizontal page matrix position between them since the overall width of the character normally assumes all seven of the available horizontal elements. The overall height of the Large Character configurations (9 elements) assume varying placements within the 14 element, 2 character position height.

Normal alphanumeric-punctuation characters are configured within a 5 x 5 element matrix embedded within the 7 x 7 matrix, thereby providing a minimum of two element positions between displayed characters. Graphics are programmed within the same 7 x 7 matrix and may assume any one or combination of elements in order to produce line diagrams and like displays.

The operator cursor character is displayed in white and turns magenta upon an interrupt service pending condition. The display configuration is that of a normal character which inverts when placed over a protected character position. The operator cursor blinks at a rate of 10 on/off cycles per second, and can be superimposed over displayed characters.

Normal and Large character configurations may be displayed in any one or combination of the following selectable attributes: any one of 8 colors (red, green, blue, yellow, cyan, white, orange, magenta), on-off blink, normal-inverted video, protect-unprotect, and normal-low intensity.



1.3 PHYSICAL DESCRIPTION

The Model 5215P-2 Display Generator (horizontal version) is housed in a standard rac-mountable chassis; the dimensions of which are 18.97 inches wide, 8.72 inches high, and 20.12 inches deep. Refer to Appendix for outline Drawing.

All internal logic circuitry is packaged on 16" x 11.5" printed circuit cards, which are edge-mounted in one row or library along the height of the chassis. EAch card may be removed from its respective card slot with the use of removal tabs located on the extreme left and right edges of the card.

Power, local control inputs and outputs, are accomplished via rear panel connections. Computer I/O connections are accomplished via rear panel mounted connectors. Wiring from the input connector to the front edge of the I/O Card TVD-193 is accomplished via cable Assembly 351-5096. Refer to Appendix for Drawing.

The total approximate weight of the Display Generator is 35 lbs.

1.4 STANDARD DISPLAY GENERATOR SPECIFICATIONS

The following list of specifications applies only to the Standard 5215 Display Generator configuration.

For Dimensions, see Outline Drawings in Appendix.

INPUT POWER*

Volts D.C.	+12V	+5V	-12V
Standard Channel Set	.500A	4.0A	.100A
I/O	.035A	3.5A	.025A
Common Logic	.035A	4.0A	.100A

TEMPERATURE RANGES

Operating	10 C to 55 C
Non-Operating	-25 C to 85 C
	10% to 95% RH (no condensation)

INTERFACE*

Standard Parallel General Purpose	9 Bit Parallel (1 parity bit/8 data bits)
I/O Transfer Rate	Up to 600K bytes/sec. Dependent on communication code type and function

CRT SCAN FORMAT

Field Rate	50Hz	Non-interlaced
Frame Rate	50Hz	
Active T.V. Lines	336	
Blanked T.V. Lines	21	
Total T.V. Lines	357	
T.V. Line Rate	17.85KHz	
Active Elements/Line	560	
Total Elements/Line	672	

CHANNEL VIDEO OUTPUT*

Number of Channels	1 to 4
Outputs per Channel	4
Red Composite Video	1
Green Composite Video	1
Blue Composite Video	1
Monochrome	1

DISPLAY CHARACTERISTICS

Normal Character Lines/Display Page	48
Normal Characters Per Character Line	80
Normal Character Matrix	
Matrix Height	7 of 336 active T.V. lines/frame
Matrix Width	7 of 560 active T.V. elements/line
Type/Number of Characters	
Control	4
Graphic	60
Alpha-numeric-punctuation	64
Large Character Matrix	
Matrix Height	14 of 336 active T.V. lines/frame
Matrix Width	7 of 560 active T.V. elements/line
Type/Number of Characters	
Alpha-numeric-punctuation (uppercase)	64
Alpha-punctuation (lowercase)	32
Greek Alphabet	32
Character Color	
All symbols except cursor	8 Selectable
Cursor Color	2 white-normal magenta-interrupt pending
Character Blink Rate	
All symbols except cursor	1 per second Duty cycle 60% ON, 40% OFF
Cursor Blink Rate	10 per second Duty cycle 60% ON, 40% OFF

*OPTIONS AVAILABLE

Chapter 2

INSTALLATION AND INTERFACING REQUIREMENTS

2.1 UNPACKING

The Model 5215 Display Generator is packaged for shipment in a custom corrugated carton.

To unpack the unit, cut the reinforced sealing tape and lift the packing material. AYDIN CONTROLS suggests that the packing material be stored for possible reshipment. Do not unpack the unit if the outer carton shows signs of damage unless the responsible shipping agent is present.

2.2 INSPECTION

Upon receipt of the unit, visually inspect the chassis for any indication of damage that may have occurred during shipment. Any damage should be reported to the responsible shipping agent. If damage is incurred, do not attempt to operate the unit unless approved by AYDIN CONTROLS.

2.3 MOUNTING

The unit requires 9" of vertical cabinet space and is designed to be mounted/supported in a standard 19" (W) rack. An adequate area must be allocated at the front and rear of the unit for interconnecting cables and connectors. The maximum depth of the unit, including installed front and rear connector mates is no longer than the overall depth of the chassis (20.12"). Mounting is accomplished with eight (8) #10-32x5/8 pan-head screws through slotted holes provided on two (2) mounting flanges.

NOTE

I/O connections are accomplished via cable-connectors at the rear of the unit. Certain options also require additional front and/or rear connector cabling. The dimensions listed in this section account for connector and connector mate dimensions only, and do not account for cable service loops or ribbon cable service folds.

2.4 CONNECTIONS AND SIGNAL DEFINITIONS

2.4.1 Video Channel Connections

Rear panel connections may be selected for associated inputs and outputs by name. Each video channel connector group is identified by channel number and provides for the following input and output connections:

CHANNEL #					
1	2	3	4	CONNECTOR NAME	FUNCTION
J1	J7	J13	J19	RED	Red Composite Video Output
J2	J8	J14	J20	GRN	Green Composite Video Output
J3	J9	J15	J21	BLU	Blue Composite Video Output
J4	J10	J16	J22	MONO	Monochrome Composite Video Output
J5	J11	J17	J23	KYBD	Display Editor Input
J6	J12	J18	J24	ALARM	Pin A Relay Contact
					B Relay Contact
					C Relay Reset (Signal In)
					D Relay Reset Return (Ground)

AYDIN CONTROLS recommends that the cable length for video/display editor connections should not exceed 300 feet (RG/59). Composite video output signal polarity conforms to EIA-STANDARD RS170.

The alarm relay output is controlled by communications codes that may be used to either set or reset the relay.

The Alarm connector may be wired to reset the relay via an external switch. The signal input is terminated with a DC resistance of 1K ohms to +5 volts in parallel with an AC load of .05µf to ground. A constant ground will hold the relay reset and when active will take priority over the communication code input which normally sets the relay.

Alarm relay specifications are as follows:

RESISTIVE LOAD MAX.	.5 AMP 50 VDC 120 VAC 10 VA
BREAKDOWN VOLTAGE	250 VDC MIN.
OPERATE TIME	1 MSEC.
CONTACT RESISTANCE	.2 Ω CLOSED 10^{10} Ω OPEN

NOTE

Contact Protection should be provided when switching other than resistance loads.

2.4.2 Sync Generator Timing Outputs

Sync Generator timing connections provide output timing and control signals for CRT compatible equipments that require synchronization timing pulses. Refer to Figure 2.4-1. Each of the connector functions is defined in the following table:

CONNECTOR NAME	FUNCTION NAME	SIGNAL DESCRIPTION
J25 CLOCK	Basic Clock	10.99MHz Element Frequency
J26 C/SYNC	Composite Sync	Horizontal Sync, Vertical Sync and Equalizing Pulse Signals
J27 C/BLANK	Composite Blanking	Horizontal and Vertical Blanking Signals
J29 H/DRIVE	Horizontal Drive	Occurs once per CRT scan line during Horizontal Retrace
J28 V/DRIVE	Vertical Drive	Occurs once per field during Vertical Retrace

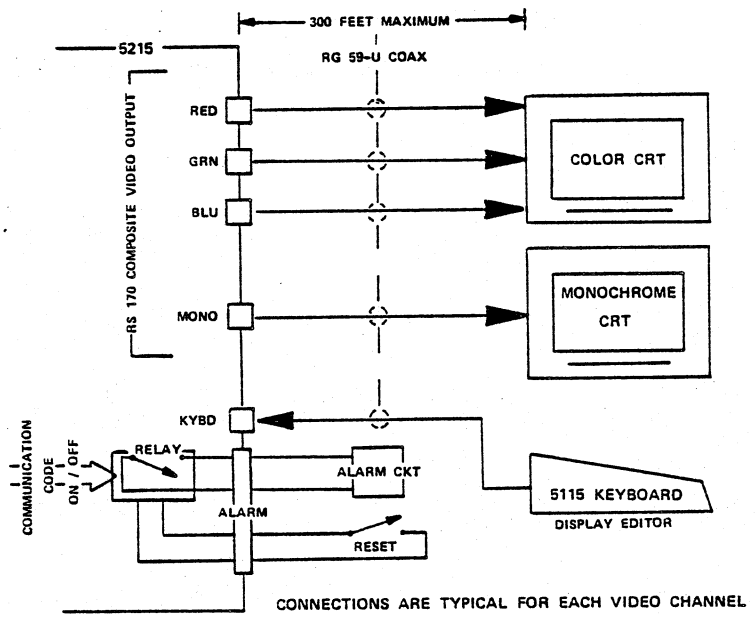
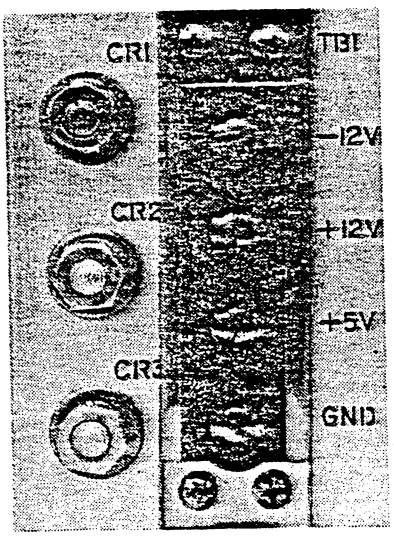


Figure 2.4-1 5215 Rear Panel Connections

2.4.3 Input Power Connections

DC power lines are connected to the unit on TB1 terminal board which is mounted on the top-left of the chassis as viewed from the rear of the unit. Four screw terminals are provided for -12VDC, +12VDC, +5VDC, and ground respectively. The following table lists the power requirements on a hardware configuration basis.



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TERMINAL NAME			LOGIC CARD GROUP	CARD TYPES
-12	+12	+5		
.100A	.035A	4.0A	Common Logic	TVD194 TVD191
.025A	.035A	3.5A	Interface	TVD193
.100A	.500A	4.0A	Each Standard Channel Set	TVD190 TVD192

2.4.4 I/O Connections and Signal Definitions

I/O signal connections are accomplished on the front edge of the TVD-193 Printed Circuit Card via a 100 pin card edge connector. Tables 2-1 through 2-4 list and define the I/O signals by name, pin location and function. Signal levels are TTL negative (ground) or positive active, as defined by a minus (-) or plus (+) sign as part of the mnemonic terms.

Interface connections are divided into two functional groups that are identified as "Computer I/O - Data/Control Bus signals", and the "5215-Priority Control Bus" signals. The Computer I/O-Data Control group includes the I/O connections that are normally associated with data transfer and interrupt signaling to and from the computer. These lines may be bussed to include multiple Display Generators on the same computer I/O port, with the limitation that the bus lines not exceed 25 feet in length. The 5215 Priority Control group includes priority and transmit/receive inhibit connections that are wired in a bus-daisy chain fashion that is local to the display subsystem.

The following illustration depicts the normal method by which the 5215 I/O and local control bus connections are configured. Subsequent paragraphs describe individual signal connections and signal levels that are required for interface connections and operations.

2.4.4.1 Computer I/O - Data Control Bus

Common computer interface configurations include a total of 23 signal lines; 12 of which are asserted by the 5215(s), and 11 of which are asserted by the computer. Individual data transfer to or from the 5215(s) is accomplished on a parallel byte basis (8 data bits and one parity bit) under control of Data Ready and Acknowledge signals.

2.4.4.2 Additional Interface Lines From Computer To 5215

Table 2-3 lists three additional lines that are available to the user to expand I/O control capabilities.

The "RESET" line, when pulsed, causes a general 5215 I/O and channel reset.

The "FORCE OFF" and "FORCE ON" lines override the 5215 communication code DG address function so as to disable/enable the receipt of data. If the F OFF+ line is not used, it must be grounded.

NOTE

The 5215 does not respond to a change in state of any of these lines with an ODA-, but rather interprets these lines to be direct switch commands.

Table 2-1

COMMON INTERFACE SIGNALS FROM 5215 TO COMPUTER

TVD-193 I/O CONNECTIONS

J33 TVD-193

PIN NO.	PIN NO.	MNEMONIC	NAME	FUNCTION
BK	17	IDB 00-	INPUT DATA BIT 0	DATA LINES FROM 5215 TO COMPUTER (8 BIT PARALLEL)
BS	18	GND		
BL	7	IDB 01-		
BT	8	GND		
BM	9	IDB 02-		
BU	10	GND		
BN	13	IDB 03-		
BV	14	GND		
BP	23	IDB 04-		
BW	24	GND		
BR	25	IDB 05-		
BX	26	GND		
BZ	11	IDB 06-		
CF	12	GND		
CA	92	IDB 07-	INPUT DATA BIT 7	
CH	91	GND		
CB	3	IDBP-	INPUT DATA BIT PARITY	PARITY BIT LINE FOR IDB 00 THROUGH IDB 07
CJ	4	GND		
CC	47	IDR-	INPUT DATA READY	INDICATES TO COMPUTER THAT IDBXX AND IDBP LINES ARE STABLE AND CONTAIN A DATA BYTE TO BE SAMPLED BY THE COMPUTER
CK	48	GND		
CD	21	IWR-	INTERRUPT WORD READY	INDICATES TO COMPUTER THAT IDBXX LINES ARE STABLE AND CONTAIN AN INTERRUPT BYTE TO BE SAMPLED BY THE COMPUTER
CL	22	GND		
CE	41	ODA-	OUTPUT DATA ACKNOWLEDGE	ISSUED IN RESPONSE TO ODR+ TO INDICATE TO THE COMPUTER THAT THE ODBXX AND ODBP LINES HAVE BEEN SAMPLED BY THE 5215. (THE COMPUTER MUST NOT CHANGE THE STATE OF THE ODBXX AND ODBP LINES UNTIL ODA IS ASSERTED.)
CM	44	GND		

NOTE

Lines are bussed in multiple 5215 configurations TTL 7438.

Table 2-2

COMMON INTERFACE SIGNALS FROM COMPUTER TO 5215

TVD-193 I/O CONNECTIONS

J33* TVD-193

PIN NO.	PIN NO.	MNEMONIC	NAME	FUNCTION
A	53	ODB 00+	OUTPUT DATA BIT 0	DATA LINES FROM COMPUTER TO 5215 (8 BIT PARALLEL)
H	54	GND		
B	90	ODB 01+		
J	89	GND		
C	86	ODB 02+		
K	85	GND		
D	88	ODB 03+		
L	87	GND		
E	98	ODB 04+		
M	97	GND		
F	100	ODB 05+		
N	99	GND		
R	84	ODB 06+		
X	83	GND		
S	94	ODB 07+	OUTPUT DATA BIT 7	
Y	93	GND		
T	96	ODBP +	OUTPUT DATA BIT PARITY	PARITY BIT LINE FOR ODB 00 THROUGH ODB 07
Z	95	GND		
V	82	ODR +	OUTPUT DATA READY	INDICATES TO 5215 THAT ODBXX AND ODBP LINES ARE STABLE AND CONTAIN A DATA BYTE TO BE SAMPLED BY THE 5215
AB	81	GND		
W	5	IDA +	INPUT DATA ACKNOWLEDGE	ISSUED IN RESPONSE TO IDR-/IWR- TO INDICATE TO THE 5215 THAT THE IDBXX AND IDBP LINES HAVE BEEN SAMPLED BY THE COMPUTER
AC	6	GND		

* Parallel Data Connections J33 Single Port and J32 used with Second Port.

Table 2-3

ADDITIONAL INTERFACE LINES FROM COMPUTER TO 5215

TVD-193 I/O CONNECTIONS

J33 TVD-193

PIN NO.	PIN NO.	MNEMONIC	NAME	FUNCTION	NOTE
AJ	37	RST-	RESET	SINGLE LINE ASSERTED BY THE COMPUTER TO RESET THE 5215 (1 MICRO-SECOND MINIMUM-PULSE)	NOT TO BE BUSSED
AE	55	F OFF+	FORCE OFF	LINE PAIR ASSERTED BY THE COMPUTER TO OVER-RIDE THE 5215 COMMUNI-CATION CODE DG ADDRESS FUNCTION	MAY BE TIED TOGETHER FOR ON/OFF SELEC-TION. CAN BE BUSSED.
AM	56	GND			
AH	43	F ON-	FORCE ON		

Table 2-4

SERIAL DATA CONNECTIONS

Signal	Connector/Pin Number
Transmit Timing	(Optional)
Transmitted Data	2 - J30/31
Received Data	3 -
Request to Send	4 -
Clear to Send	5 -
Data Set Ready	6 -
Signal Ground	7 -
Data Carrier Detected	8 -
Chassis Ground	1 - J30/31

SERIAL DATA CONNECTIONS (J30 AND J31)

Chapter 3

CONTROLS AND INDICATORS

3.1 INTRODUCTION

This chapter includes detailed functional descriptions relating to the Model 5215 Display Generator controls (switches) and indicators.

3.2 MANUAL CONTROLS

Other than 5215 compatible Display Editors (keyboards) and associated external cursor control device (Light Pen), no other local controls are provided except for one manual pushbutton (S1) located at the front bottom-left corner of the 5215 chassis.

Depressing this pushbutton switch causes an initialize-clear of 5215 through the following sequential firmware-hardware operations:

1. Hardware clear of timing and control circuits.
2. Initialization of the control card program and associated display generator hardware.
3. Initialization of the Symbol Status Register to white-normal attributes.
4. Clear of all video channel displays with the automatic writing of black, normal attributes spaces, followed by the writing of a green, inverted, blinking, normal size "I" at the top left extreme of the CRT display(s).
5. Clear of all video channel Interrupt Registers, Interrupt Mask Registers, and Memory Mask Registers.
6. Clear of DG Interrupt Register.
7. Clear of DG Interrupt Mask Register.

3.3 ILLUMINATING INDICATORS

One illuminating indicator (DS1) is provided on the rear of the unit to indicate the absence of the required DC voltages. When the proper DC power levels are present on a voltage detect circuit, the indicator illuminates (green). When any one or combination of voltages is absent or at an improper voltage level, the indicator is extinguished.

Chapter 4

HARDWARE

THEORY OF OPERATION

4.1 INTRODUCTION

This chapter includes a general presentation of all standard 5215 Display Generator hardware operations.

The 5215 Engineering Drawings (Volume II, Document AR94-V-EDWG) are required in order to support the text included herein. References to the associated Block Diagrams and Data Flow Charts are included within the text.

Section 4.2 references the Master Block Diagram for an overall description of the standard logic card functions and the basic logic operations that are associated with each card.

4.2 STANDARD LOGIC CARD FUNCTIONS AND BASIC LOGIC CIRCUIT OPERATIONS

The Master Data Flow Block Diagram in Volume II, depicts the Standard 5215 Printed Circuit Card data bus interconnections and the basic logic circuit functions within each card. The following text describes these circuit functions on an individual P.C. card-circuit basis.

4.2.1 Sync Generator Card TVD-191 (Reference Block 1)

The Sync Generator Circuits provide the timing signals required to synchronize the various inter-related functions of the display generator.

All timing is derived from a basic clock oscillator that operates at 10.99MHz. The basic clock frequency is further divided into lower frequencies and timing frames by a ÷7 Element Shift Register and other dedicated timing circuits. Timing outputs are presented to the TVD-194 Control Card, TVD-190 Video Card, TVD-192 Edit Card, and TVD-193 I/O Card.

4.2.1.1 CRT Data/Scan Control Logic

The basic clock frequency may be directly related to display element (dot) times, each of which is approximately 90ns.

The Element Shift Register divides this frequency by 7 to produce a timing reference relative to horizontal Page Matrix Symbol positions.

The CRT Data/Scan Control Logic utilizes the element Shift Register output and dividing circuits to produce horizontal data scan line, symbol line, and Page Matrix display field time frames.

CRT Scan Control signals are synchronized with data timing to cause the CRT beam to move so as to produce a data frame of 336 CRT scan lines in which element data is displayed.

4.2.1.2 RAM Memory Timing

The RAM Memory Timing provides memory cycle timing pulses to control the 4K x 15 Refersh Random Access Memory located on the TVD-190 card. Individual memory cycles are dedicated to the separate functional operations of: I/O display data transfers, the editing of existing memory data and the refresh display of RAM memory data to the CRT.

4.2.1.3 Refresh Address

The display operation (refresh) address source is generated on the TVD-191 card and is control linked to the refresh memory cycle timing to produce dedicated refresh memory accesss cycles. The refresh address value is supplied to the Refresh RAM memory via the TVD-192 card.

4.2.1.4 Control Card Cycle Logic

The Control Card Cycle Logic timing controls Byte Processor and Program Memory operations that occur on the TVD-194 card. Since some processor operations (I/O and Edit) are dependent on the Random Access Memory (TVD-190 as a data source or destination, the Control Card Cycle Logic is control linked to operate outside of the refresh memory cycle timing (paragraphs 4.2.1.2 and 4.2.1.3). Control card and channel set operations are also linked to I/O operations via these timing signals.

4.2.2 Control Card TVD-194 (Reference Block 3)

The Control Card controls and performs the majority of I/O transfers and data manipulation operations that occur to and from the Display Generator. Display writing, reading, and the editing of existing displays is performed by an internal processor program that is accessed via communication codes and code sequences.

4.2.2.1 Byte Processor and Comparator

Data Transfers to the Byte Processor occur via the Source Bus. Included within the processor are an Arithmetic-Logic Unit (ALU), a Buffer Memory, and an Accumulator to perform mathmatical, logical, and compare test operations.

4.2.2.2 Program Memory

The Program Memory contains the Display Generator fixed control program in a 1K x 16 Programmable Read Only memory. A Program Counter addresses the memory sequentially under control of Control Card Cycle Timing from the TVD-191 card. The Prom output may be transferred to the Processor or channel set via the I/O Source Multiplexer and Source Bus as dictated by prom program instructions.

4.2.2.3 Instruction Decode

The Instruction Decode circuitry receives Instruction Register outputs to subsequently decode instructions for data transfers, data manipulation, or hardware functions. The Data Transfer circuitry selects source to destination data paths and controls data destination load pulses. The Flag Circuitry is normally used as a base by which the processor program tests on or controls display generator hardware conditions.

4.2.2.4 Comparator

The Comparator Circuit Compare Register is loaded from the Source Bus under control of TVD-194 program instruction in order to compare a predetermined value with a value placed on the Bus as read from the channel set. When a comparison is detected via the Compare circuitry, a flag is set for further test by the processor (paragraph 4.2.2.3).

4.2.2.5 Channel Address Select

The Channel Address Select logic includes an Address Register, which when loaded via the Source Bus or Keyboard Encoder, selects the channel set as a data source and/or destination. Data transfer from the Source Bus to the selected channel set is accomplished via line drivers that are included as part of this circuit.

4.2.2.6 DG Symbol Status Register

The DG Symbol Status Register is loaded from byte 1 of the Source Bus under control of a TVD-194 program instruction to identify the attributes of display character configurations. Once loaded, the DG Symbol Status Register data is normally transferred to byte 2 of the Source Bus for further transfer to Refresh Ram (TVD-190). A transfer of this type normally occurs in parallel with byte 1 of the Source Bus, the value of which represents a display character configuration in ASCII form.

4.2.3 Video Card TVD-190 (Reference Block 4)

The Video Card is one of the two printed circuit cards that constitute the Standard Channel Set, and is the central data flow point within the channel set for refresh, edit and I/O operations.

4.2.3.1 Channel Data Source Multiplexer

The Channel Data Source Multiplexer selects any one of four data inputs to the Channel Source Bus under control of TVD-194 program instructions.

4.2.3.2 Refresh RAM Memory

The 4K x 15 Random Access Memory's primary function is to retain character display data for CRT refresh purposes. Read/Write memory cycle timing is supplied to the RAM from the TVD-191 card for the purpose of reading data from the memory for display (refresh) and to the I/O card to develop Reply Messages to the computer. The RAM is also accessed for display update, edit, and other internal control operations. Addresses are supplied to the RAM on a functional basis via the TVD-192 card.

The Memory Buffer Register is a one memory word storage cell that provides a link between the RAM and the Output Data Multiplexer.

The Insert Delete Register is an additional memory word storage cell dedicated to inser/delete edit operations, and is linked back to the RAM through the Channel Data Source Multiplexer for edit operations.

The Output Data Multiplexer selects either the Memory Buffer Register of a compatible keyboard (display editor) as the source of data transfer to the Bus. Normally, the Memory Buffer Register is placed on the Bus for development of Reply Messages via the I/O card, whereas Display Editor data is normally tested by the processor via the Source Bus Multiplexer for control and edit functions.

4.2.3.3 Video Logic

The Video Logic accepts data directly from the Ram and converts memory data to display configurations on a display character line-per character line basis.

RAM data is stored in the Data Storage circuitry which is further converted to CRT compatible data through the Data Generation circuits. The Data Output Circuits combine CRT scan control signals

with CRT serial data to form the required input to an RS170 level compatible RGB color or monochrome CRT monitor.

4.2.4 Edit Card TVD-192 (Reference Block 5)

The Edit Card's primary functions are to support memory access operations within the Standard Channel Set and to maintain channel interrupt data storage.

4.2.4.1 Refresh RAM Address Logic

Within the Refresh RAM Address Logic are three counter-registers, the values of which are supplied to the Refresh Memory via the X-Y Address Multiplexer and Menu Rotate Logic.

The Cursor XY counter values become the memory address when writing or reading individual Page Matrix character positions.

The Multifunction and Special Function counters are used as internal control address values, the functions of which are determined by the TVD-194 program.

The Refresh Address from the TVD-191 card is selected as the RAM address via the X and Y address multiplexer to support CRT refresh operations (paragraph 4.2.3.2).

Under control of the TVD-194 card, the XY Cursor Counters, and Multifunction Counter may be placed on the Bus.

4.2.4.2 Channel Interrupt Logic

The Channel Interrupt Logic circuits store and report new channel interrupts to the TVD-193 card. Interrupts are normally generated by the transfer of an interrupt bit oriented word to the Interrupt Status Register and Interrupt Storage Register from the keyboard via the Source Bus. The Interrupt Status Register data would subsequently be transferred to the computer via the Edit Register Multiplexer, Bus, and I/O card when commanded by a TVD-194 program instruction.

4.2.4.3 Currsor Display Comparator

The Cursor Display Comparator compares the normally static output of the XY Cursor Counters (paragraph 4.2.4.1) with the output of the dynamic Refresh Address Counters to signal to the TVD-190 card Video Logic that the operator's cursor character is to be displayed.

4.2.4.4 Memory Mask Register

The Memory Mask Register output is presented to the TVD-190 Refresh RAM to prevent changes in the memory during RAM access when editing display data. This register is loaded via the Source Bus under control of a TVD-194 program instruction.

4.2.4.5 Function Decode Control

Byte oriented instructions or TVD-194 instruction control lines effect the Function Decode and control circuits to cause edit card counter and hardwired logic operations.

4.2.4.6 Keyboard Data Receive Control Logic

A compatible operator keyboard inputs directly to a channel set via this circuitry. The serial bit pattern developed by the keyboard is interpreted within this logic to activate control lines which signal the Display Generator that data is present for input from the keyboard. Serial data is channeled via this circuit to the TVD-190 card to be converted to parallel compatible data for further use by the TVD-190, TVD-192, or TVD-194 cards.

4.2.5 I/O Card TVD-193 (Reference Block 2)

The I/O card provides the necessary data and control link between the Display Generator Control Card and the Computer. All data transfers are accomplished under control of the TVD-194 card in a parallel fashion to and from the TVD-194 Source Bus via this card.

4.2.5.1 Receive Logic

As each byte is transferred to the I/O logic, the data is stored in the Data In Register for test by the Parity Error Detect circuits. Data is subsequently transferred to the Source Bus via the Source Bus Multiplexer for direct transfer to a destination that is determined by the TVD-194 program or communication code configuration.

4.2.5.2 Transmit Logic

Data Transfer source from the Display Generator to the computer is accomplished under control of the TVD-194 card program.

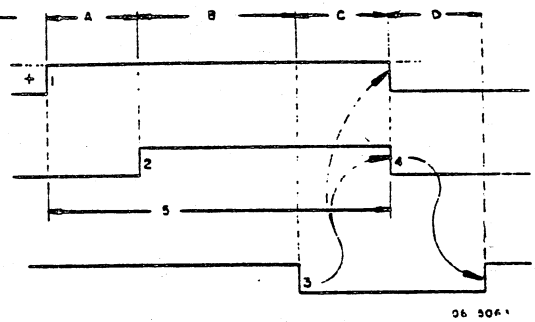
Data is presented to the I/O card from the Source Bus for subsequent transfer to the computer via the Output Multiplexer. As each byte is transferred to the computer, a byte parity bit is added via the Parity Generator circuit. The Status Change Circuitry compares previously transferred Refresh Memory Data display status (attributes) with current transfers in order to report such changes in the output data stream.

The Display Generator Address Register is normally loaded via the Source Bus on an incoming data transfer if the Display Generator is to be addressed for communication purposes. The Display Generator Address Register and the Display Generator Interrupt Registers may be placed on the Output Data Lines via the Output Multiplexer.

4.2.5.3 Data Transfer Timing - Computer to 5215

The following timing diagram depicts a typical single data byte transfer operation from the Computer to the 5215; references to related signal sources are included. ODB 00+ through ODB P+ and ODR+ are controlled by the computer. ODA- is controlled by the Display Generator.

	LOGIC PAGE NO.	COMPONENT ID	COMPONENT/ CIRCUIT NAME
TVD-193 I/O	3	U51 U52	ODB 00 THRU 07 & ODB P
	3	U55	ODR +
	3	U27	ODA -



1 COMPUTER ASSERTS ACTIVE ODB+ LINES

2 COMPUTER ASSERTS ODR+

3 DISPLAY GENERATOR ASSERTS ODA- AFTER SAMPLING ODB LINES AND CAUSES ODR+ TO NEGATE

4 ODR+ NEGATION CAUSES ODA- TO NEGATE

5 ODB+ LINES MUST REMAIN IN STABLE STATE FOR A THRU C TIME DURATION

A TIME - MIN = 100NS
MAX = COMPUTER CONTROLLED

B TIME - MIN = 1μSEC
MAX = 5MSEC DEPENDING ON DATA TYPE

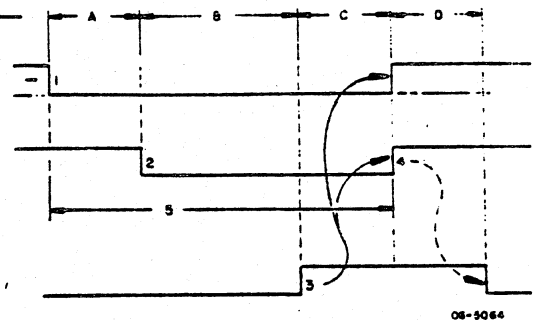
C TIME - MIN = PROPAGATION DELAY
MAX = COMPUTER CONTROLLED

D TIME = PROPAGATION DELAY

4.2.5.4 Data Transfer Timing 5215 to Computer

The following timing diagram depicts a single data byte transfer operation from the 5215 to the computer; References to related signal sources are included. IDB 00- through IDB P-, IDR- and IWR- are controlled by the 5215. IDA+ is controlled by the computer.

	LOGIC PAGE NO.	COMPONENT ID	COMPONENT/ CIRCUIT NAME
TVD-193 I/O	1	U68 U69	IDB 00 THRU 07 & IDB P
	1	U66	IDR - OR IWR -
	1	U39	IDA +



1 DISPLAY GENERATOR ASSERTS ACTIVE IDB- LINES

2 DISPLAY GENERATOR ASSERTS IDR-

3 COMPUTER ASSERTS IDA+ AFTER SAMPLING IDB LINES AND CAUSES IDR- TO NEGATE

4 IDR- NEGATION CAUSES IDA+ TO NEGATE

5 IDB- LINES REMAIN IN STABLE STATE FOR A THRU C TIME DURATION
IDB- LINES CHANGE 400NS BEFORE THE NEXT SEQUENTIAL IDA+

* IWR- CAN BE ASSERTED DURING A COMPUTER TO DISPLAY GENERATOR DATA TRANSFER

A TIME - MIN = 300NS
MAX = 400NS

B TIME - MIN = PROPAGATION DELAY
MAX = COMPUTER CONTROLLED

C TIME = PROPAGATION DELAY

D TIME - MIN = PROPAGATION DELAY
MAX = COMPUTER CONTROLLED
NEXT SEQUENTIAL IDR- CANNOT BE ASSERTED UNTIL IDA+ IS NEGATED

Chapter 5

MAINTENANCE

5.1 INTRODUCTION

This chapter contains general corrective and preventative maintenance requirements, and procedures for the 5215 Display Generator. Documentation referencing conventions are included.

WARNING
ALL PRECAUTIONS REGARDING SAFETY MUST BE FOLLOWED WHEN HANDLING OR MAINTAINING THIS UNIT. ALTHOUGH THERE ARE NO VOLTAGES IN EXCESS OF 120VAC PRESENT IN THE UNIT, INDUSTRY ESTABLISHED PRECAUTIONS SHOULD BE STRICTLY ADHERED TO FOR BEST PERSONNEL SAFETY AND EQUIPMENT UTILIZATION.

5.2 TEST EQUIPMENT AND TOOL REQUIREMENTS

One each, known good, PWB for the DG.

5.3 PREVENTIVE MAINTENANCE

Preventive maintenance is limited to cleaning, inspection, and periodic diagnostic test.

5.3.1 Cleaning

Non-corrosive solutions such as common soap and water. are recommended as outside chassis cleaning agents.

CAUTION
POWER SHOULD BE DE-ENERGIZED WHEN CLEANING THE UNIT. NO LIQUID IS TO ENTER THE UNIT IN ANYWAY SINCE OPERATIONAL FAILURES MAY OCCUR DUE TO ELECTRICAL SHORTS.

AYDIN CONTROLS recommends that the user vacuum clean all other surfaces as required to remove dust particles and other foreign materials.

5.3.2 Inspection

Physical inspection of rear connector panel cabling is suggested to ensure against wear such as fraying or cuts.

Strain relief assemblies should be inspected for a firm grip on the outer insulation of the attached cable, but not so tight so as to crimp the internal conductors. Connectors should maintain a firm seating and lock.

CAUTION
REMOVING CONNECTORS FOR ORDINARY INSPECTION IS NOT RECOMMENDED, SINCE PROGRESSIVE DETERIORATION MAY OCCUR.

Printed circuit card assembly locations should be inspected for total assembly seating in their respective

5.3.3 Diagnostic Tests

AYDIN CONTROLS recommends that an I/O diagnostic test be performed on the unit at least once per month. The HPV-2 Subsystem Test Program, No. 51191033, provides the tests as described in Section 8.2 of the HPV-2 Subsystem Maintenance Manual, 4400AR94-M.

5.4 CORRECTIVE MAINTENANCE

Corrective maintenance for microprogrammed equipment such as the 5215 can become very complicated if a fault analysis is to be taken to the logic element level. It is for this reason that AYDIN CONTROLS recommends that the user base corrective maintenance on faulty I.C. card replacement in lieu of specific logic element replacement for first line troubleshooting.

CAUTION
IF REMOVAL/REPLACEMENT OF THE TVD-194 IS NECESSARY, REMOVE THE TVD-193 I/O CONNECTOR FIRST OR DAMAGE TO TVD-194 PROMS MAY RESULT.
PRIMARY POWER SHOULD BE DE-ENERGIZED PRIOR TO P. C. CARD REMOVAL OR REPLACEMENT

5.5 RECOMMENDED SPARE PARTS

AYDIN CONTROLS recommends that a spares stocking level of ten percent (10%) of the total equipment purchased be considered with a minimum stocking quantity of one (1) for each P.C. card or system type.

5.6 DETAILED PHYSICAL DESCRIPTION AND REFERENCING CONVENTIONS

The text and illustrations included within this section define physical hardware identification methods and engineering drawing/support diagram referencing conventions.

5.6.1 Horizontal Configuration

All internal logic circuitry is packaged on 16" x 11.5" printed circuit boards, which are edge-mounted in one row or library along the height of the chassis. Refer to Figures 5.6.1-1 and 5.6.1.2-1. Each card may be removed from its respective card slot with the use of removal tabs located on the extreme left and right edges of the card. Each card is identified as to its card type by an identification number located on the right removal tab. The card positions (slots) of the card library are numbered from bottom to top as viewed from the front of the unit. All cards must be inserted with the component sides of the cards facing up as viewed from the front of the unit.

Potentiometers used in conjunction with adjustments are accessible from the front of the unit, and are located on the open card edges of the associated printed circuit cards. Internal circuit card logic circuits and discrete electronic components are accessed for dynamic test purposes with the use of a plug-in type extender card.

Printed circuit card interconnecting wiring, and chassis card connectors are located toward the rear of the unit, accessible by removing two screws on the left side of the jack panel and swinging jack panel to the right. The card library contains two eighty-six pin chassis mounted card connectors for each associated circuit card. The right group of connectors are identified as J1, and the left group of connectors are identified as J2. All chassis mounted card connector pins are divided into two horizontal rows. The row located on the top contains even numbered pins (2-86), the row located beneath contains odd numbered pins (1-85). The card slots (associated connector locations) are numbered from top to bottom 1 through 13 as viewed from computer input connections to the Display Generator for the various input configurations as shown in Figure 5.6.1.2-1, A through D.

P.C. CARD TYPE	CARD NAME IDENTIFICATION	CARD SLOT
TVD-192	EDIT	13
	vid chan 1	
TVD-190	VIDEO OUTPUT	12
TVD-192	EDIT	11
	vid chan 2	
TVD-190	VIDEO OUTPUT	10
TVD-192	EDIT	9
	vid chan 3	
TVD-190	VIDEO OUTPUT	8
TVD-192	EDIT	7
	vid chan 4	
TVD-190	VIDEO OUTPUT	6
TVD-191	SYNC GENERATOR	5
TVD-194	MICROPROCESSOR (CONTROL)	4
TVD-193	I/O	3

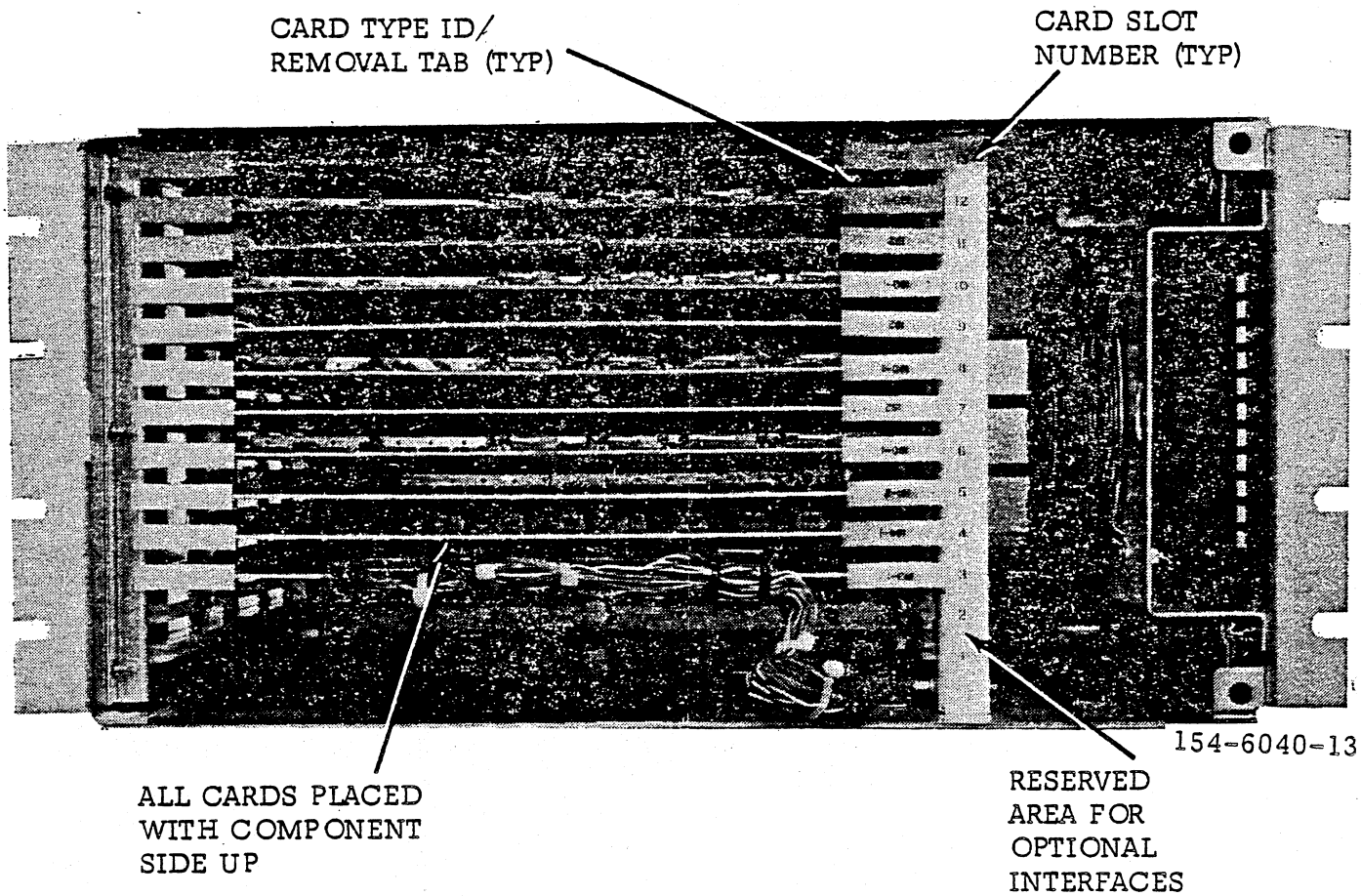


Figure 5.6.1-1 Printed Circuit Card Identification And Locations

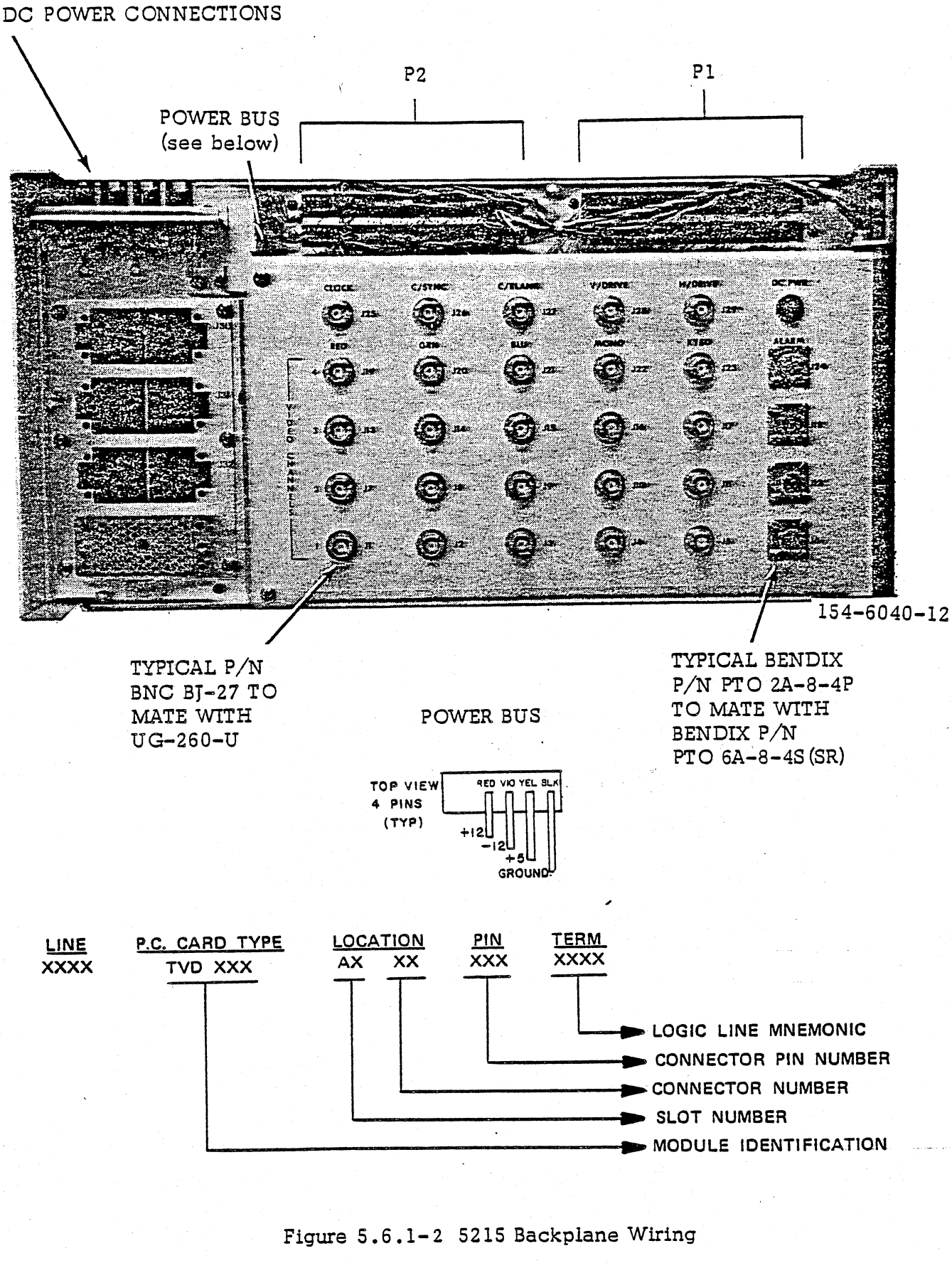


Figure 5.6.1-2 5215 Backplane Wiring

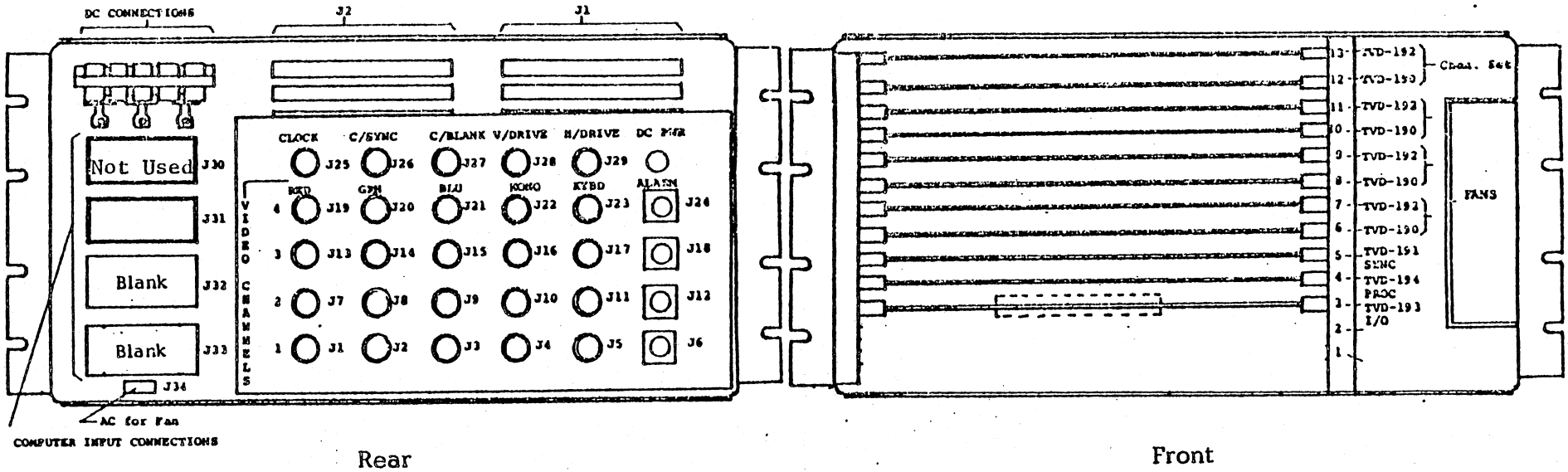


Figure 5.6.1.2-1A Outline For Single Asynchronous Modem, Serial Input

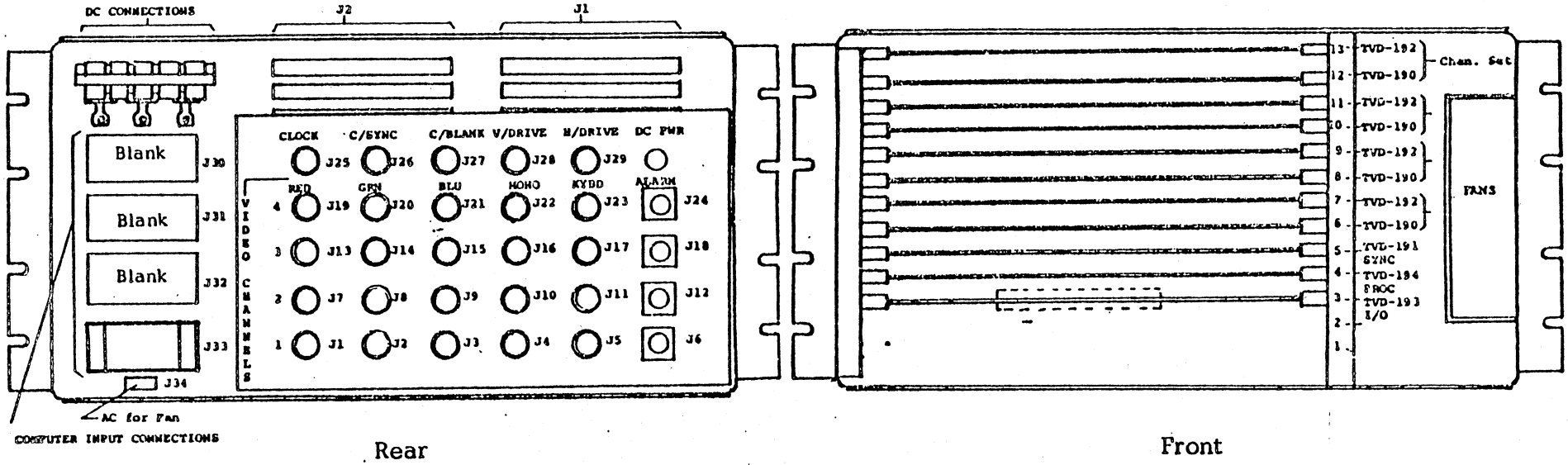


Figure 5.6.1.2-1B Outline For Single Computer, Parallel Input

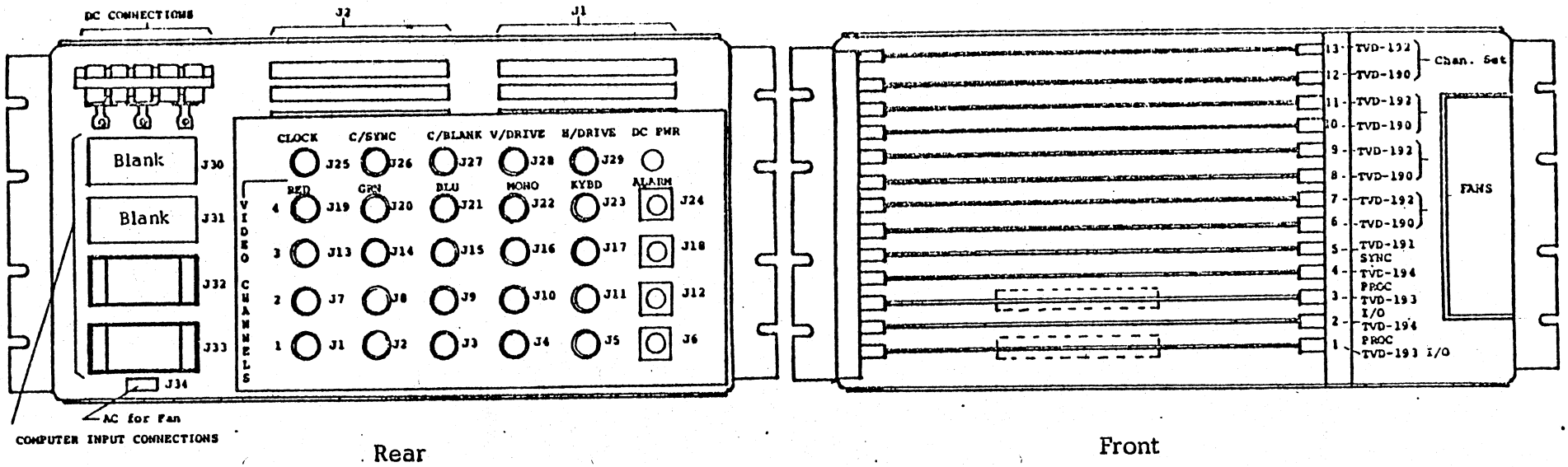


Figure 5.6.1.2-2C Outline For Dual Computer, Parallel Input

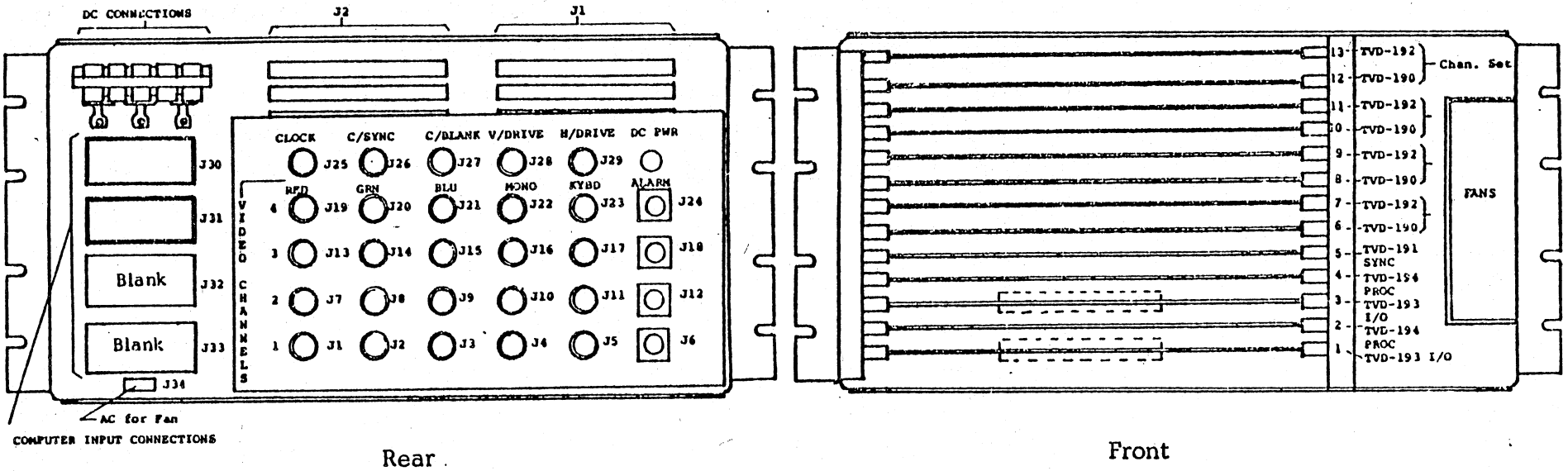


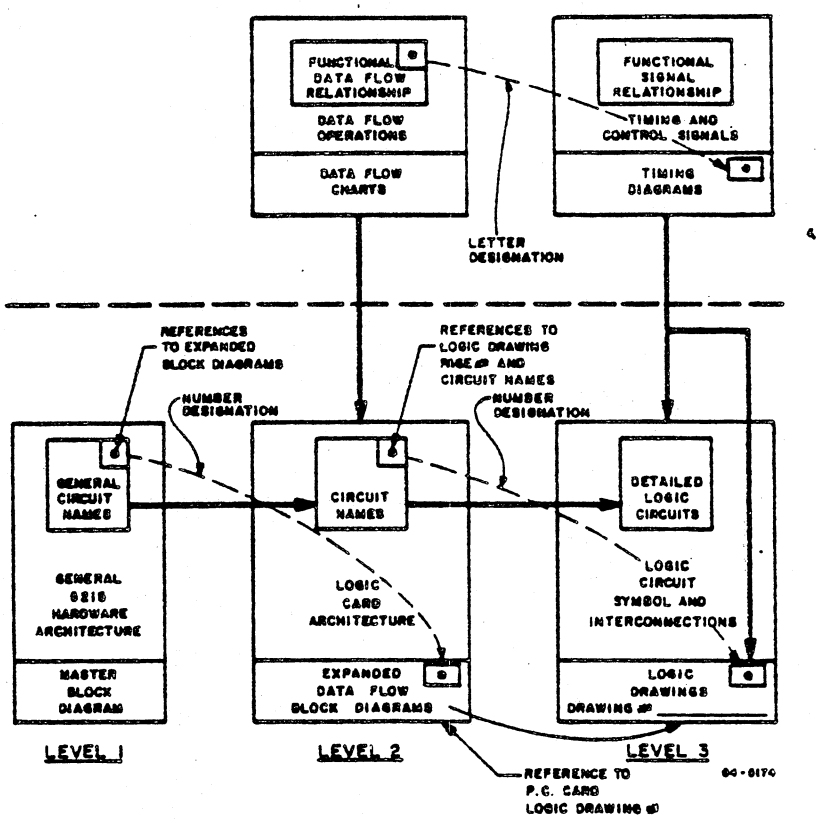
Figure 5.6.1.2-2D Outline For Dual Asynchronous Modem, Serial Input

5.6.2 Support Diagram/Illustration Cross Reference Methods

Supporting engineering diagrams and illustrations define the 5215 hardware operations utilizing a "three level" method of documentation. Illustration references include a Master Block Diagram (level 1) which is keyed via reference number-on a logic card basis-to Expanded Block Diagram (level 2). The expanded block diagrams are further keyed to associated engineering logic drawings via logic drawing number, page number, and individual circuit name (level 3).

Data Flow Charts provide a functional description of Block Diagram data flow operations with references to individual circuit names. Data Flow Charts are directly referenced to Timing Diagrams via letter designation.

Timing Diagrams support timing generation and control flow with direct references to logic drawing source page number, component I.D., circuit name and component name.



5.6.3 Adjustments

5.6.3.1 Video Amplifiers

This adjustment compensates for single video element versus contiguous video element display characteristics. Refer to Figure 5.6.3-1.

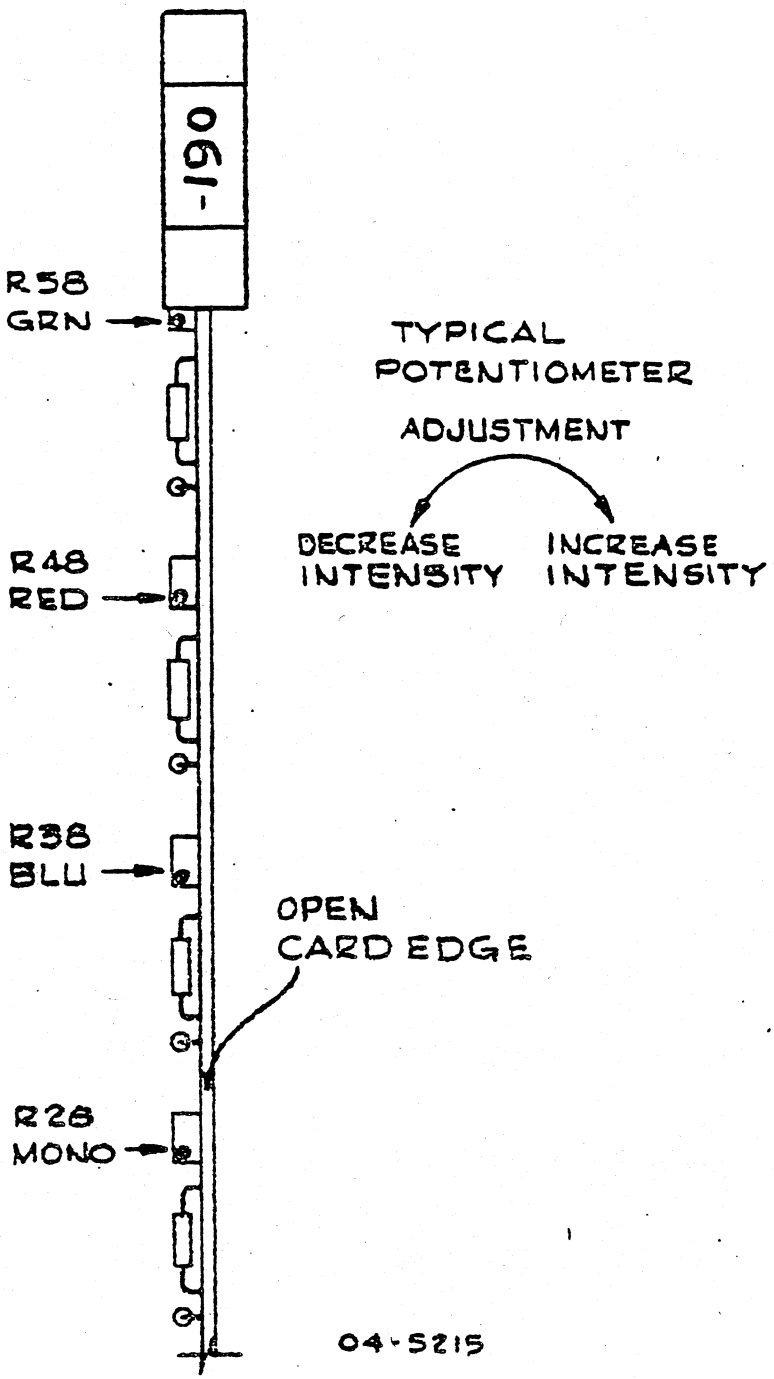


Figure 5.6.3-1 Video Adjustments

Through the changing of potentiometer resistive values, contiguous video pulses other than single and/or first video pulses will increase/decrease in amplitude, thereby balancing video intensity between horizontal and vertical CRT display lines.

The potentiometers that are associated with this adjustment procedure are located on the TVD-190 open card edge(s). Four TVD-190 adjustments are required for each associated video channel output (i.e., red, blue, green, mono.).

Perform the operations and adjustments for each of four video channels as listed and defined in the following procedure:

Repeat (1) and (2) on each of four keyboards.

(1) Depress and release each of the following keyboard keys:

A) WHITE

B) BKGD-NOR

C) SIZE-NOR

D) BLINK-OFF

E) INTENSITY-FULL

(2) Write a full page of "T" characters by depressing FAST HORIZ RPT and "T" keyboard keys simultaneously.

Repeat (3), (4), (5) and (6) for each TVD-190 PC card.

(3) Blank all but green video (CRT switches) on each video channel. While viewing the Video Channel CRT, adjust R (green) potentiometer until the video intensity of the horizontal crossbars of the "T" characters equal the intensity of the vertical lines of the "T" characters.

(4) Blank all but red video (CRT switches) on each video channel. While viewing the Video Channel CRT, adjust R (red) potentiometer until the video intensity of the horizontal crossbars of the "T" characters equal the intensity of the vertical lines of the "T" characters.

(5) Blank all but blue video (CRT switches) on each video channel. While viewing the Video Channel CRT, adjust R (blue) potentiometer until the video intensity of the horizontal crossbars of

"T" characters equal the intensity of the vertical lines of the "T" characters.

(6) Connect the mono output of the DG to the green input of the nRT.

(7) Blank all but green video.

(8) While viewing the Video Channel CRT, adjust R (mono) potentiometer until the video intensity of the horizontal crossbars of the "T" characters equal the intensity of the vertical lines of the "T" characters.

Chapter 6

OPTIONS

6.1 INTRODUCTION

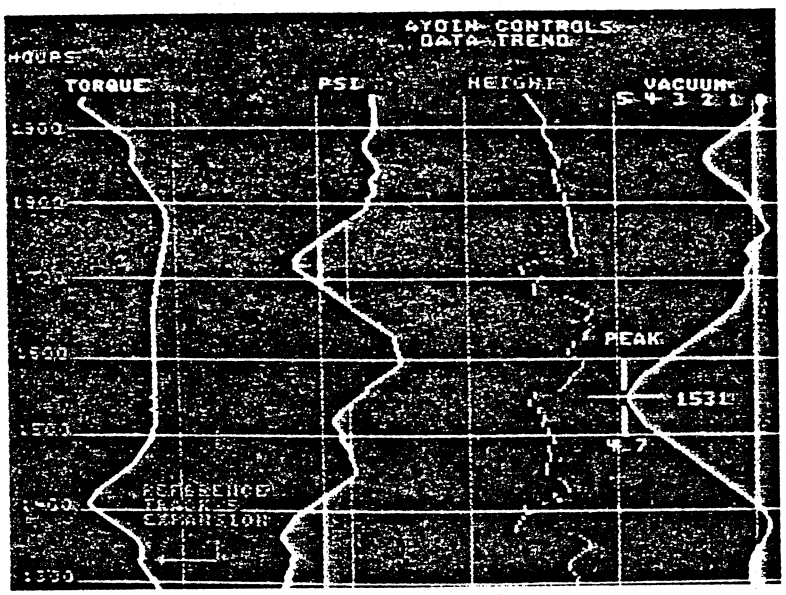
This chapter contains text and tables that define hardware options that may or may not apply to the user's Display Generator configuration.

6.2 DESCRIPTION OF ASYNCHRONOUS MODEM INTERFACE

This section describes the Asynchronous Modem Interface to the 5215 Display Generator. The ASM interface can transmit and receive data at rates from 75 baud to 9600 baud. The bit rate is selectable by means of DIP switches located on the TVD-193 card. All line drivers and receivers are RS232 compatible. The serial data word consists of a start bit, 8 data bits, a parity bit, and a stop bit. Serial data is low true, and all control lines are high true. Refer to table 6.2-1 for location of signals. If the user provides an external bit rate clock, the DG will transmit data on the falling edge of the external clock.

TABLE 6.2-1 SERIAL I/O CONNECTIONS

Signal	Connector/Pin Number
Transmit Timing	(Optional)
Transmitted Data	2 - J30/31
Received Data	3 -
Request to Send	4 -
Clear to Send	5 -
Data Set Ready	6 -
Signal Ground	7 -
Data Carrier Detected	8 -
Chassis Ground	1 - J30/31



6.3 DATA TREND CHANNEL SET

The AYDIN CONTROLS Model 5215-DTCS Data Trend Channel Set provides enhanced operation of the Model 5215 Display Generator by providing a means to display up to four channels of Trend Data in a format which is similar to a strip chart recorder. The Data Trend Channel Set generates the actual data plots, time lines, and amplitude grid, while alphanumeric notation is provided by a standard Model 5215-CS Channel Set. The output of the Data Trend and Standard Channel Set are "OR'd" on the Data Trend and presented to a single CRT. No specialized interfaces are required since the Data Trend shares the common channel interface of the display generator. Up to four Data Trend Channel Sets can be installed in each Model 5215 Display Generator. They are addressed the same as a Standard Channel Set.

The update rate of the display is determined by the computer and the time scale can be programmed to represent seconds, minutes, days, months, or years as required by the application. Data is displayed on one of four tracks along with a horizontal time line per track, and automatically advances from top to bottom as each new data point is received. The resolution of the display is 512 elements in the horizontal direction (chart lines) by 256 elements in the vertical direction. Vertical amplitude lines are displayed in green with every fifth line intensified. The spacing is uniform across the picture and determined by the computer so that the amplitude scale can be varied. The spacing between amplitude lines can be any integer number up to 16 resolution elements.

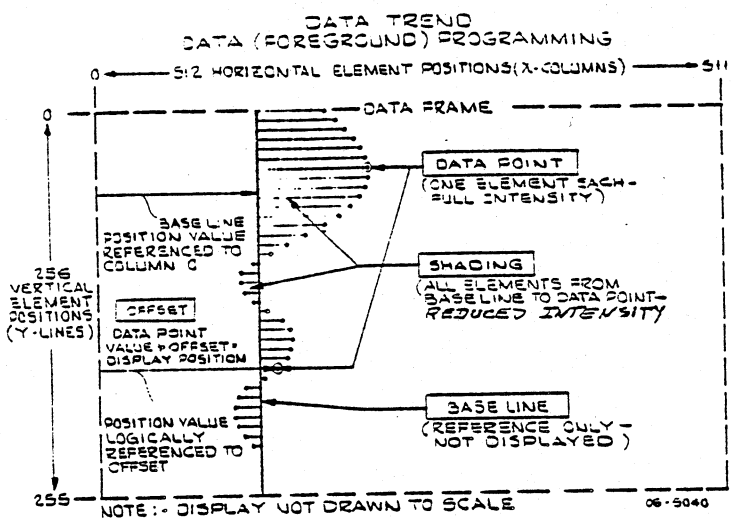
Time line programming allows for time scale references to be presented in a visual format that is representative of the users application. Time lines are entered on YO and are displayed from the left limit to the right limit for each track. As each new data point is written on the display, all previous entries are advanced to the next sequential vertical element position. Time lines will automatically move with each new data point so that the time reference is always correct.

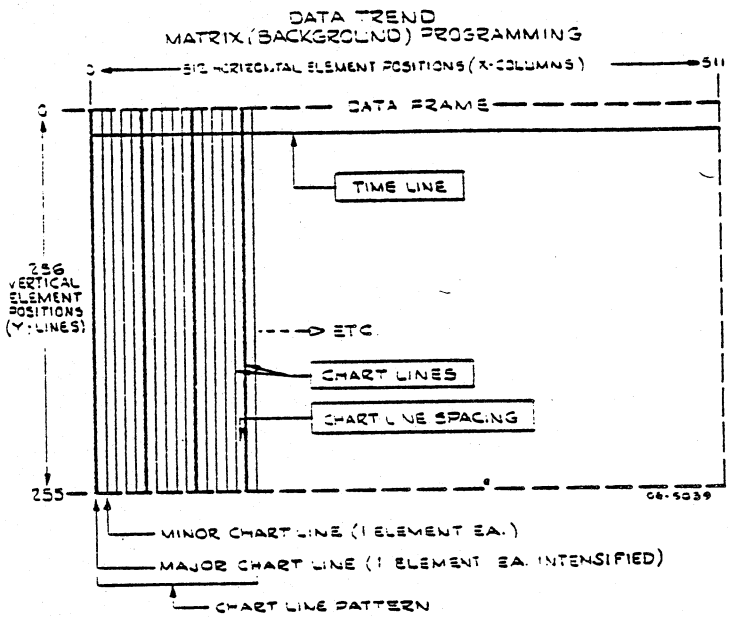
Data points are program entered at YO in any one of four data tracks, each of which is associated with one of four colors, i.e., white, yellow, magenta and cyan. As each new data point is written, all previous data points and time line entries within the data track are shifted down to the next sequential vertical element display position.

An offset value can be program assigned and stored for each data track. This value is then added to each data point thereby providing greater flexibility in overall data track horizontal positioning. Data track presentations may be shifted on the display without requiring computer software to recalculate the positions of display data points.

Base line and shading enhance the presentation of waveforms, graphs, and like formats by providing a base line to data point visual reference. The base line value can be programmed for each of the four available data tracks. When shading is specified, all element positions from the assigned base line value to the data track's data points are illuminated at reduced intensity. Over and under limits may also be specified for each track. The space between the limits and the data point is shaded in red whenever the over or under limit is exceeded.

Under limit should be programmed as "0" and over limit should be programmed "511" whenever it is desired to eliminate the limit check. Note that the actual resolution for specifying limits is one part in 256 since the LSB bit is used to specify lower or upper limits. The lower limit appears on even resolution elements while the upper limit appears on odd resolution elements.





6.3.1 Data Trend Theory Of Operation

The majority of the display information for the Data Trend is contained within 2 RAMS (Random Access Memories). Refer to the Data Trend block diagram (6), in Volume II. Detailed drawings of the Data Trend Channel Set PCB subassemblies, TVD-195 and TVD-196 are also included in Volume II.

The larger RAM is segmented into four parts of 256 addressable words. Each word is eleven bits wide. Nine of the eleven bits are used for an absolute Data Point value from Ø up thru 511. The tenth bit is used as a flag to indicate whether the Data Point is to be illuminated on the CRT. This bit (the Video bit) is used mainly for an internal clear of an entire track. The eleventh bit is the Time Line bit. All 256 Data Points on all four tracks may have a Time Line.

The smaller RAM is also segmented into four parts (one part for each track). Each part contains four values: Offset, Baseline Address, Left Limit Address, and Right Limit Address. The outputs of this RAM are loaded directly into the Left Limit counters and the Right Limit counters for each track.

During the loading of all counters, both RAMS are addressed by a synchronous counter which also is decoded to provide for sixteen load pulses for the counters. The offset value from the 16 x 9 RAM is arithmetically added to the Data Point value from the 1k X 11 RAM and the result loaded into the Data Point counters during the appropriate time slots. If the resultant value after the addition is greater than 511, a value of 511 is loaded into the Data Point counter. The Video bit is loaded into the Data Point counters to disable the data value in the event that the Data Points are not to be displayed.

Data from the 16 x 9 RAM is loaded into the baseline counters in addition to the Video bit from the 1k X 11 RAM. The loading of the Video bit disables any shading in the event that a Data Point is not to be displayed.

All counters are loaded from the RAMS during horizontal blanking, and count down to zero as the electron beam sweeps across the CRT from left to right. When zero is reached in any counter, additional circuitry is activated to affect the display (i.e. illuminate a Data Point, turn off shading, turn shading from track color to red, etc.). As the counters are decrementing to zero, the RAMS are free to be updated by the computer.

6.3.2 Data Trend Specifications

Computer Input	- Same as specified for the 5215 Display Generator (NOTE: Data entered as though it were a cursor coordinate while control codes are entered as though they were Channel Status Mask codes).
Video Signals	- All video signal timing and impedance are in accordance with EIA-RS170 STANDARD. The output is the "OR" of the alphanumeric and Data Trend Channels.
Video Outputs	- Red and Sync 1 BNC Connector Green and Sync 1 BNC Connector Blue and Sync 1 BNC Connector Monochrome and Sync 1 BNC Connector
Relay Closure	- Print command from the computer causes a relay to set/reset which can be used to cause a hardcopy device (external) to record the present picture.
Display Format	- Track #1 Graphic Data White Track #2 Graphic Data Yellow Track #3 Graphic Data Magenta Track #4 Graphic Data Cyan
Refresh Memory	- Semiconductor.
Number of Tracks	- Four per channel - up to four channels per Display Generator.
Resolution	- 512 resolution elements per line. 256 lines per page (Maximum depends on 5215 picture format).
Base Line	- Programmable per track.
Upper/Lower Limits	- Programmable per track.
Offset	- Programmable per track.
Amplitude Lines	- Programmable per display with up to 16 resolution elements separation.
Power Requirements	- Each set requires 2.4A at +5 volts, 160ma at +12 volts.

Mechanical Configuration	- Two cards which require two card slots in the 5215 Display Generator TVD 195, 196.
Environment	- Operating temperature: 10°C to 45°C. Non-operating temperature: 25°C to 85°C. Humidity: 10% to 95% RH (no condensation)